

## **REMARKS**

After entry of this amendment, claims 1-19 are pending in the application. Claim 1 has been amended, while claims 18 and 19 have been added. In the present office action, claims 1-9 were rejected under 35 U.S.C. § 102(e) as being anticipated by Clift, U.S. Patent 6,633,970. Claims 10-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Clift in view of Buti, U.S. Patent 6,421,758. Applicant respectfully traverses these rejections and respectfully requests reconsideration.

### **35 U.S.C. § 102(e) Rejection:**

Applicant respectfully submits that independent claim 1 and associated dependent claims 2-9 recite combinations of features not taught or suggested in Clift. Independent claim 1 recites, in pertinent part:

“a plurality of addressable units, each addressable unit addressed by a different logical register name (LRN) to which that addressable unit is statically assigned ... and a control circuit coupled to the plurality of addressable units wherein the control circuit is configured, responsive to a new PRN being assigned to a first LRN that addresses a first addressable unit of the plurality of addressable units, to cause the current PRN in the first storage location of the first addressable unit to be copied to a second storage location which is one of the other storage locations of the first addressable unit, wherein the second storage location corresponds to a current checkpoint of a plurality of checkpoints” (Emphasis added).

Clift does not teach or suggest this combination of features. More particularly, does not teach a memory wherein each of a plurality of addressable units is addressed by a different LRN to which that addressable unit is statically assigned. In viewing Fig. 5 and its associated text in the specification, it is clear that history buffer entries are not statically assigned to a logical register. In column 15, lines 45-65, Clift states:

“Step 2 of FIG. 5 illustrates the result of issuing uop u0 (i.e., allocating an[d] RF entry and updating primary array 110 and history buffer 122) according to an

example embodiment of the present invention. As shown in the list of uops 505, uop u0 is a write to logical register A. At allocation time for uop u0, the allocator 120 allocates the next available RF entry as the Pdst for u0. In this case, the next available RF entry is RF6. After the RF entry (RF6) is selected for the uop u0, the RAT 108 reads out the old RF entry pointer (to RF1) in primary array 110 for register A, and stores this old RF entry pointer in the free/old field 312 of the first entry of history buffer 122, shown in FIG. 5 as line 520. The newly allocated RF pointer (pointer to RF6) is then stored in the new field 310 for this entry in the history buffer 122, shown as line 522. An A is written to the logical destination field 314 for uop u0 to indicate that logical register A is being renamed or mapped to physical register RF6. The retirement field 316 for u0 is cleared to a zero (0) and will remain cleared until uop u0 retires. The RAT primary array 110 is then updated to store the pointer to the new RF entry (RF6) allocated to register A, shown as line 524.” (Emphasis added).

The operation is further described in the remainder of Col. 15 and in Col. 16.

From the above citation, as well as in Fig. 5, it is clear that the history buffer entries taught by Clift are not statically assigned to a logical register. Further, with regard to history buffer 122 of Clift, it is clear that any free entry therein may be assigned to any logical register, and that such assignments are transitory and tied to a sequence of instructions. Accordingly, Clift cannot teach or suggest “a plurality of addressable units, each addressable unit addressed by a different logical register name (LRN) to which that addressable unit is statically assigned ... and a control circuit coupled to the plurality of addressable units wherein the control circuit is configured, responsive to a new PRN being assigned to a first LRN that addresses a first addressable unit of the plurality of addressable units, to cause the current PRN in the first storage location of the first addressable unit to be copied to a second storage location which is one of the other storage locations of the first addressable unit, wherein the second storage location corresponds to a current checkpoint of a plurality of checkpoints” (Emphasis added).

For at least the above-stated reasons, Applicant respectfully submits that claim 1 and its associated dependent claims are patentably distinct over Clift, as Clift does not teach or suggest all of the elements recited therein. Accordingly, removal of the 35 U.S.C. § 102(e) rejection of claims 1-9 is respectfully requested.

**35 U.S.C. § 103(a) Rejection:**

Applicant respectfully submits that independent claim 10 and associated dependent claims 11-17 recite combinations of features not taught or suggested in the alleged combination of Clift and Buti. Independent claim 10 recites, in pertinent part:

“a plurality of memory locations, each corresponding to a different physical register name (PRN), and wherein each memory location is configured to store a logical register name (LRN) and a plurality of valid indications, and wherein each of the valid indications corresponds to a checkpoint and is indicative of whether or not the PRN is assigned to the LRN at that checkpoint”

Neither Clift nor Buti, taken singly or in combination, teach or suggest a plurality of valid indications each corresponding to a checkpoint and which are indicative of whether or not a PRN is assigned to a given LRN at that checkpoint. The present office action states that a plurality of valid indications is taught by Clift in Fig. 5, Ref. 316. In Col. 7, line 61 to Col. 8, line 3, Clift states:

“The Retire field 316 is a 1 if the uop has been executed and retired, thereby making the old RF entry free to be reallocated for a new uop. If the retire field 316 is a 1, the corresponding free/old field 312 indicates a "free" (or available) RF entry. If the retire field 316 is a 0 (meaning the uop and old RF entry are not yet retired), then XXX/New field 310 will refer to a new RF entry (a new Pdst) and the free/old field 312 will refer to an old RF entry (an old Pdst) because the old RF entry is not yet free (available).”

From the above citation, it is clear that the retire field does not correspond to a valid checkpoint or indicate that a given PRN is assigned to a given LRN for that checkpoint. Rather, the retire field 316, as stated in the above citation, is used to indicate whether or not a uop for a given RF entry is retired or not. Furthermore, neither Clift nor Buti provides any teaching or suggestion of any type of indication corresponding to a checkpoint that is indicative of whether or not a given PRN is assigned to a given LRN. Accordingly, Applicant respectfully submits that the cited references, taken singly or in combination, do not teach or suggest all of the elements of independent claim 10, and thus a case of obviousness has not been established. Applicant thus respectfully requests removal of the 35 U.S.C. § 103(a) rejection of claims 10-17.

**Patentability of the Added Claims:**

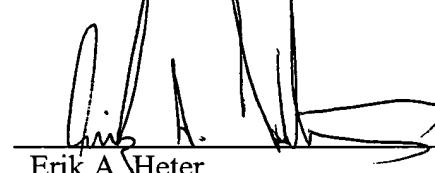
The present amendment adds claims 18 and 19. Applicant submits that no new matter has been added, and that the claims are fully supported in the application as filed. For example, claim 18 is supported by Fig. 5B and its associated text in the specification, while claim 19 is supported by Fig. 5A and its associated text. Claims 18 and 19 each depend from independent claim 1, and are thus believed allowable for at least the reasons stated above in regard thereto.

**CONCLUSION**

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-90000/EAH.

Respectfully submitted,

  
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